Amendment to the Claims

This listing of Claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (Currently Amended) A liquid crystal display device comprising:

a plurality of pairs of gate lines including first and second gate lines adjacent to each other;

a plurality of data lines perpendicular to the first and second gate lines, thereby defining a plurality of left and right side pixel regions; and

left and right side pixel electrodes, respectively formed in the left and right side pixel regions, and selectively driven by ~~switching parts~~ switching-parts of the first and second gate lines, respectively,

wherein each of the left and right side pixel electrodes overlaps greater than one gate line.

2. (Original) The liquid crystal display device of claim 1, wherein the first and second gate lines of one pair of gate lines respectively drive the left and right side pixel electrodes connected with the same data line.

3. (Original) The liquid crystal display device of claim 1, wherein the left and right side pixel electrodes are overlapped with a preceding or corresponding pair of the gate lines.

4. (Original) The liquid crystal display device of claim 3, wherein the right side pixel electrode is overlapped with the first and second gate lines of the preceding pair, and the left side pixel electrode is overlapped

with the first gate line of the corresponding pair and the second gate line of the preceding pair.

5. (Original) The liquid crystal display device of claim 4, wherein storage capacitors are formed at an overlapping portion between the left or right side pixel electrode and each gate line.

6. (Original) The liquid crystal display device of claim 3, wherein the left side pixel electrode is overlapped with the first and second gate lines of the preceding pair, and the right side pixel electrode is overlapped with the first gate line of the corresponding pair and the second gate line of the preceding pair.

7. (Original) The liquid crystal display device of claim 6, wherein storage capacitors are formed at an overlapping portion between the left or right side pixel electrode and each gate line.

8. (Original) The liquid crystal display device of claim 1, further comprising a plurality of source drive ICs, a number of source drive ICs equal to a number of colors in each pixel region times a number of data lines divided by twice a number of outputs in each source drive IC.

9. (Original) The liquid crystal display device of claim 1, further comprising a plurality of the gate drive ICs, each gate drive IC having a plurality of scanning signal output terminals, each scanning signal output terminal corresponding to a particular pair of the pairs of the gate lines and supplying a scanning signal to the particular pair; and

a plurality of the selection parts, each selection part time-dividing the scanning signal output from a particular scanning signal output terminal of one of the gate drive ICs and selectively applying the time-divided scanning signal to the first or second gate line of the particular pair.

10. (Original) The liquid crystal display device of claim 9, wherein the display device is an XGA class display which contains 1536 data lines and 1536 gate lines.

11. (Original) The liquid crystal display device of claim 10, wherein if a picture is transmitted at 60Hz, a selection block of a scanning signal applied to each gate line is about 10.85μs.

12. (Original) The liquid crystal display device of claim 10, wherein if a picture is transmitted at 60Hz, a selection block of a scanning signal applied to each gate line is about 21.7μs.

13. (Original) The liquid crystal display device of claim 10, wherein exactly 6 gate drive ICs are provided, each gate drive IC having 256 pins.

14. (Original) The liquid crystal display device of claim 10, wherein exactly 3 gate drive ICs are provided, each gate drive IC having 256 pins.

15. (Original) The liquid crystal display device of claim 10, further comprising exactly four source drive ICs, each source drive IC having 384 pins.

16. (Original) The liquid crystal display device of claim 9, further comprising a plurality of source drive ICs, a number of the source drive ICs smaller than a number of the gate drive ICs.

17. (Currently Amended) A liquid crystal display device comprising:

a plurality of pairs of gate lines, each pair of gate lines including first and second gate lines adjacent to each other;

a plurality of data lines perpendicular to the pair of the first and second gate lines, thereby defining a plurality of left and right side pixel regions;

left and right side pixel electrodes, respectively formed in the left and right side pixel regions, and selectively driven by ~~switching parts~~ switching-parts of the first and second gate lines, respectively,

a gate drive IC having a scanning signal output terminal corresponding to one of the pairs of the gate lines, the scanning signal output terminal supplying a scanning signal; and

a selection part time-dividing the scanning signal output from the gate drive IC and selectively applying the time-divided scanning signal to the first or second gate line of the one of the pairs of the gate lines,

wherein each of the left and right side pixel electrodes overlaps greater than one gate line.

18. (Original) The liquid crystal display device of claim 17, wherein the scanning signal output from the gate drive IC is divided into a first signal and a second signal which are then applied to the first and second gate lines, respectively.

19. (Original) The liquid crystal display device of claim 17, wherein the selection part includes:

a first selection switch activated by a first clock signal to apply the scanning signal to the first gate line of the one of the pairs of gate lines; and

a second selection switch activated by a second clock signal having a phase difference of 180° with respect to the first clock signal, the

second clock signal applying the scanning signal to the second gate line of the one of the pairs of gate lines when activated.

20. (Original) The liquid crystal display device of claim 17, wherein the selection part includes:

a first logic circuit that combines the scanning signal and a first clock signal, an output of the first logic circuit connected with the first gate line of the one of the pairs of gate lines; and

a second logic circuit that combines the scanning signal and a second clock signal, the second clock signal having a phase difference of 180° with respect to the first clock signal, the first logic circuit connected with the second gate line of the one of the pairs of gate lines.

21. (Original) The liquid crystal display device of claim 17, wherein the selection part includes:

a first AND gate receiving and logically combining the scanning signal and a first clock signal, then outputting the combination to the first gate line of the one of the pairs of gate lines; and

a second AND gate receiving and logically combining the scanning signal and a second clock signal having a phase difference of 180° with respect to the first clock signal, then outputting the combination to the second gate line of the one of the pairs of gate lines.

22. (Original) The liquid crystal display device of claim 17, further comprising a plurality of source drive ICs, a number of source drive ICs equal to a number of colors in each pixel region times a number of data lines divided by twice a number of outputs in each source drive IC.

23. (Original) The liquid crystal display device of claim 17, further comprising a plurality of the gate drive ICs, each gate drive IC having a plurality of scanning signal output terminals, each scanning signal output

terminal corresponding to a particular pair of the pairs of the gate lines and supplying a scanning signal to the particular pair; and

a plurality of the selection parts, each selection part time-dividing the scanning signal output from a particular scanning signal output terminal of one of the gate drive ICs and selectively applying the time-divided scanning signal to the first or second gate line of the particular pair.

24. (Original) The liquid crystal display device of claim 23, wherein the display device is an XGA class display which contains 1536 data lines and 1536 gate lines.

25. (Original) The liquid crystal display device of claim 24, wherein if a picture is transmitted at 60Hz, a selection block of a scanning signal applied to each gate line is about 21.7μs.

26. (Original) The liquid crystal display device of claim 24, further comprising exactly four source drive ICs, each source drive IC having 384 pins.

27. (Original) The liquid crystal display device of claim 23, further comprising a plurality of source drive ICs, a number of the source drive ICs smaller than a number of the gate drive ICs.

28. (Currently Amended) A liquid crystal display device comprising:

a plurality of sets of adjacent gate lines;

a plurality of data lines perpendicular to the gate lines;

a plurality of sets of pixel regions, each set of pixel regions containing at least two pixel regions and bounded by adjacent data lines and, at furthest, gate lines most distal from each other in adjacent sets of

the sets of the adjacent gate lines, no pixel region overlapping any other pixel region; and

a plurality of sets of pixel electrodes, each pixel electrode disposed in a particular pixel region and overlapping greater than one gate line,

wherein at least one pixel electrode of adjacent pixel electrodes either overlaps at least two gate lines of one of the sets of adjacent gate lines or overlaps one of the gate lines of a first set of the sets of adjacent gate lines and one of the gate lines of a second set of the sets of adjacent gate lines.

29. (Original) The liquid crystal display device of claim 28, wherein adjacent pixel electrodes overlap different gate lines.

30. (Original) The liquid crystal display device of claim 28, wherein each pixel electrode overlaps exactly two gate lines.

31. (Currently Amended) The liquid crystal display device of claim 28, wherein the at least one pixel electrode of adjacent pixel electrodes overlaps the at least two gate lines of one of the sets of adjacent gate lines.

32. (Currently Amended) The liquid crystal display device of claim 28, wherein the at least one pixel electrode of adjacent pixel electrodes overlaps the one of the gate lines of a first set of the sets of adjacent gate lines and the one of the gate lines of a second set of the sets of adjacent gate lines.

33. (Original) The liquid crystal display device of claim 28, wherein each set of adjacent gate lines comprises exactly two adjacent gate lines.

34. (Original) The liquid crystal display device of claim 28, further comprising a plurality of storage capacitors, each storage capacitor formed by the overlap between one of the pixel electrodes and one of the gate lines.

35. (Original) The liquid crystal display device of claim 28, further comprising:

a gate drive IC having a scanning signal output terminal corresponding to at least one of the sets of adjacent gate lines, the scanning signal output terminal supplying a scanning signal; and

a selection part time-dividing the scanning signal output from the gate drive IC and selectively applying the time-divided scanning signal to the gate lines of the one of the sets of adjacent gate lines.

36. (Original) The liquid crystal display device of claim 35, wherein the scanning signal output from the gate drive IC is divided into a plurality of output signals and each output signal is supplied to a different gate line of the one of the sets of gate lines.

37. (Original) The liquid crystal display device of claim 35, wherein the selection part includes a plurality of selection switches which are each activated at different, non-overlapping times.

38. (Original) The liquid crystal display device of claim 37, wherein the selection switches are activated by different clock signals.

39. (Original) The liquid crystal display device of claim 35, wherein the selection part includes a plurality of logic circuits which are each activated at different, non-overlapping times.

40. (Original) The liquid crystal display device of claim 39, wherein each logic circuit combines the scanning signal and a different clock signal of a plurality of clock signals.

41. (Original) The liquid crystal display device of claim 40, wherein the logic circuits are AND gates.

42. (Original) The liquid crystal display device of claim 35, wherein the one of the sets of adjacent gate lines includes exactly two gate lines: a first gate line and a second gate line.

43. (Original) The liquid crystal display device of claim 42, wherein the selection part includes:

a first AND gate receiving and logically combining the scanning signal and a first clock signal, then outputting the combination of the scanning signal and the first clock signal to the first gate line; and

a second AND gate receiving and logically combining the scanning signal and a second clock signal having a phase difference of 180° with respect to the first clock signal, then outputting the combination of the scanning signal and the second clock signal to the second gate line.

44. (Original) The liquid crystal display device of claim 28, further comprising a plurality of source drive ICs, a number of source drive ICs equal to (a number of colors in each pixel region times a number of data lines) divided by (a number of outputs in each source drive IC times a number of adjacent gate lines in each set of the adjacent gate lines).

45. (Original) The liquid crystal display device of claim 28, further comprising a plurality of gate drive ICs, each gate drive IC having a plurality of scanning signal output terminals, each scanning signal output terminal corresponding to a particular set of the sets of the gate lines and supplying a scanning signal to the particular set; and

a plurality of selection parts, each selection part time-dividing the scanning signal output from a particular scanning signal output terminal of one of the gate drive ICs and selectively applying the time-divided scanning signal to one of the gate lines of the particular set.

46. (Original) The liquid crystal display device of claim 28, further comprising a plurality of gate drive ICs supplying signals to the gate lines and a plurality of source drive ICs supplying signals to the data lines, wherein a number of the source drive ICs is smaller than a number of the gate drive ICs.

47. (Currently Amended) A method of fabricating a liquid crystal display device, the method comprising:

forming a plurality of sets of adjacent gate lines;

forming a plurality of data lines perpendicular to the gate lines; and

forming a plurality of sets of pixel electrodes, each set of pixel electrodes containing at least two pixel electrodes, each set of pixels bounded by adjacent data lines and, at furthest, gate lines most distal from each other in adjacent sets of the sets of the adjacent gate lines, each pixel electrode overlapping greater than one gate line and no pixel electrode overlapping any other pixel electrode,

wherein at least one pixel electrode of adjacent pixel electrodes either overlaps at least two gate lines of one of the sets of adjacent gate lines or overlaps one of the gate lines of a first set of the sets of adjacent gate lines and one of the gate lines of a second set of the sets of adjacent gate lines.

48. (Original) The method of claim 47, further comprising forming the pixel electrodes such that adjacent pixel electrodes overlap different gate lines.

49. (Original) The method of claim 47, further comprising forming the pixel electrodes such that each pixel electrode overlaps exactly two gate lines.

50. (Currently Amended) The method of claim 47, ~~further comprising forming the pixel electrodes such that~~ wherein the at least one pixel electrode of adjacent pixel electrodes overlaps the at least two gate lines of one of the sets of adjacent gate lines.

51. (Currently Amended) The method of claim 47, ~~further comprising forming the pixel electrodes such that~~ wherein the at least one pixel electrode of adjacent pixel electrodes overlaps the one of the gate lines of a first set of the sets of adjacent gate lines and the one of the gate lines of a second set of the sets of adjacent gate lines.

52. (Original) The method of claim 47, further comprising forming the gate lines such that each set of adjacent gate lines comprises exactly two adjacent gate lines. (Original)

53. (Original) The method of claim 47, further comprising forming a plurality of storage capacitors, each storage capacitor formed by the overlap between one of the pixel electrodes and one of the gate lines.

54. (Original) The method of claim 47, further comprising connecting a scanning signal output terminal of a gate drive IC with at least one of the sets of adjacent gate lines, the scanning signal output terminal supplying a scanning signal, time-dividing the scanning signal output from the gate drive IC using a selection part, and selectively applying the time-divided scanning signal to the gate lines of the one of the sets of adjacent gate lines.

55. (Original) The method of claim 54, further comprising dividing the scanning signal output from the gate drive IC into a plurality of output signals and supplying each output signal to a different gate line of the one of the sets of gate lines.

56. (Original) The method of claim 54, further comprising activating each of a plurality of selection switches of the selection part at different, non-overlapping times.

57. (Original) The method of claim 56, further comprising activating the selection switches using different clock signals.

58. (Original) The method of claim 54, further comprising activating each of a plurality of logic circuits of the selection part at different, non-overlapping times.

59. (Original) The method of claim 58, further comprising providing the logic circuits such that each logic circuit combines the scanning signal and a different clock signal of a plurality of clock signals.

60. (Original) The method of claim 59, further comprising providing AND gates as the logic circuits.

61. (Original) The method of claim 54, further comprising forming the gate lines such that the one of the sets of adjacent gate lines includes exactly two gate lines: a first gate line and a second gate line.

62. (Original) The method of claim 61, further comprising receiving and logically combining the scanning signal and a first clock signal and then outputting the combination of the scanning signal and the first clock signal to the first gate line using a first AND gate, and receiving and logically combining the scanning signal and a second clock signal

having a phase difference of 180° with respect to the first clock signal and then outputting the combination of the scanning signal and the second clock signal to the second gate line using a second AND gate.

63. (Original) The method of claim 47, further comprising connecting a number of source drive ICs equal to (a number of colors in each pixel region in which each pixel electrode is formed times a number of data lines) divided by (a number of outputs in each source drive IC times a number of adjacent gate lines in each set of the adjacent gate lines) with the data lines.

64. (Original) The method of claim 47, further comprising connecting a plurality of scanning signal output terminals of a plurality of gate drive ICs with the gate lines, each scanning signal output terminal corresponding to a particular set of the sets of the gate lines, and supplying a scanning signal to the particular set, and time-dividing the scanning signal output from a particular scanning signal output terminal of one of the gate drive ICs and selectively applying the time-divided scanning signal to one of the gate lines of the particular set using one of the selection parts of a plurality of selection parts.

65. (Original) The method of claim 47, further comprising connecting a plurality of gate drive ICs with the gate lines and a plurality of source drive ICs with the data lines, a number of the source drive ICs smaller than a number of the gate drive ICs.

66. (Currently Amended) A method of decreasing manufacturing cost of a liquid crystal display device, the method comprising:

obtaining a liquid crystal display panel comprising:

a plurality of sets of adjacent gate lines;

a plurality of data lines perpendicular to the gate lines; and

a plurality of sets of pixel electrodes, each set of pixel electrodes containing at least two pixel electrodes, each set of pixels bounded by adjacent data lines and, at furthest, gate lines most distal from each other in adjacent sets of the sets of the adjacent gate lines, no pixel electrode overlapping any other pixel electrode, wherein at least one pixel electrode of adjacent pixel electrodes either overlaps at least two gate lines of one of the sets of adjacent gate lines or overlaps one of the gate lines of a first set of the sets of adjacent gate lines and one of the gate lines of a second set of the sets of adjacent gate lines;

obtaining a plurality of gate drive ICs and a plurality of source drive ICs; and

connecting the gate drive ICs with the gate lines and source drive ICs with the source lines.